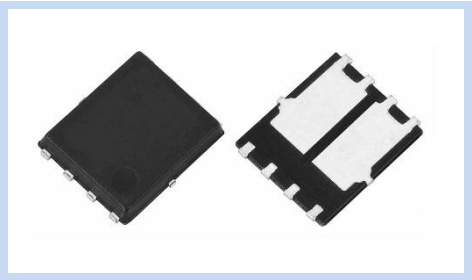
Dual N-Channel MOSFET AEC-Q101
60V 16A 25W DFN5×6-8L

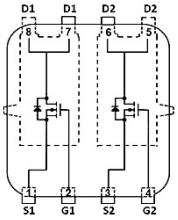
MFT62N16D56A

MERITEK

FEATURE

- $R_{DS(ON)}$<50mΩ, V_{GS}=10V, I_D=8A
- $R_{DS(ON)}$ <60mΩ, V_{GS}=4.5V, I_D=4A
- Low On-Resistance
- Low Imput Capacitance
- Application: DC-DC Converter, Switching Power Supply, High-Side Load Switching, Motor Control
- AEC-Q101 Qualified





RoHS

MECHANICAL DATA

- Case: DFN5×6-8L Package
- Terminals: Solderable per MIL-STD-750, Method 2026

MAXIMUM RATINGS

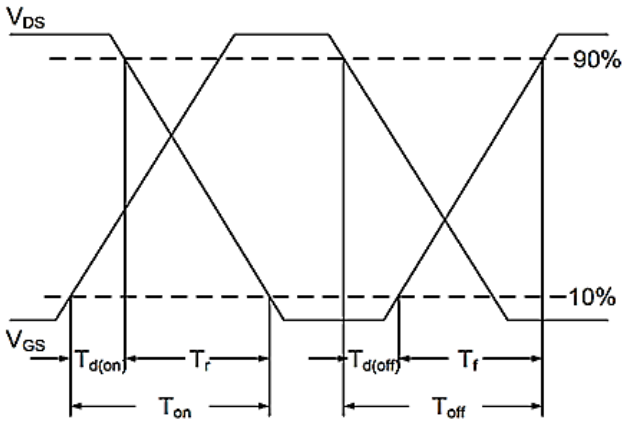
Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current – Continuous	T_C= 25°C	I_D	16	A
	T_C= 100°C		12	
Drain Current – Pulsed	T_C= 25°C	I_{DM}	64	A
Power Dissipation	T_C= 25°C	P_D	25	W
	T_C= 100°C		12.5	
Drain Current – Continuous	T_A= 25°C	I_D	5	A
	T_A= 70°C		4.5	
Power Dissipation	T_A= 25°C	P_D	2.5	W
	T_A= 70°C		1.8	
Single Pulse Avalanche Energy		E_{AS}	1.6	mJ
Thermal Resistance Junction to Case		$R_{\theta JC}$	6	°C/W
Thermal Resistance Junction to Ambient		$R_{\theta JA}$	60	°C/W
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to +175	°C

ELECTRICAL CHARACTERISTICS

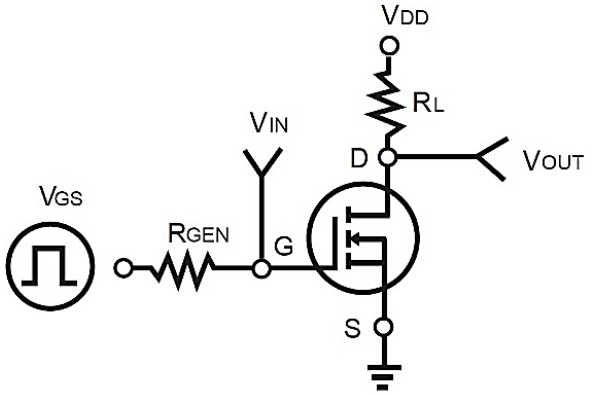
Off Characteristics	Conditions	Symbol	Min	Typ.	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250μA	BV_{DSS}	60	--	--	V
Drain-Source Leakage Current	V_{DS}=60V, V_{GS}=0V,	I_{DSS}	--	--	1	μA
Gate-Source Leakage Current	V_{GS}=±20V, V_{DS}=0V	I_{GSS}	--	--	±100	nA
On Characteristics	**Conditions**	**Symbol**	**Min**	**Typ.**	**Max**	**Unit**
Static Drain-Source On-Resistance	V_{GS}=10V, I_D=8A	$R_{DS(ON)}$	--	34	50	mΩ
	V_{GS}=4.5V, I_D=4A		--	38	60	
Gate Threshold Voltage	V_{GS}=V_{DS} , I_D=250μA	$V_{GS(th)}$	1.0	1.7	2.5	V
Dynamic Characteristics	**Conditions**	**Symbol**	**Min**	**Typ.**	**Max**	**Unit**
Total Gate Charge	V_{DS}=48V, V_{GS}=10, I_D=8A	Q_g	--	13	--	nC
Gate-Source Charge		Q_{gs}	--	2.1	--	
Gate-Drain Charge		Q_{gd}	--	2.9	--	
Turn-On Delay Time	V_{DS}=48V, V_{GS}=10V, R_G=3Ω, I_D=8A	$T_{d(on)}$	--	8.4	--	ns
Rise Time		T_r	--	33	--	
Turn-Off Delay Time		$T_{d(off)}$	--	32	--	
Fall Time		T_f	--	27	--	
Input Capacitance	V_{DS}=30V , V_{GS}=0V , F=1MHz	C_{iss}	--	609	--	pF
Output Capacitance		C_{oss}	--	43	--	
Reverse Transfer Capacitance		C_{rss}	--	14	--	
Gate Resistance	F=1MHz	R_g	--	3.7	--	Ω
Drain-Source Body Diode	**Conditions**	**Symbol**	**Min**	**Typ.**	**Max**	**Unit**
Diode Forward Current	T_C= 25°C	I_S	--	--	16	A
Pulse Diode Forward Current		I_{SM}	--	--	64	
Diode Forward Voltage	V_{GS}=0V , I_S=1A	V_{SD}	--	0.72	1.0	V
Reverse Recovery Time	I_S=8A, V_{GS}= 0V, dI_S/dt=100A/μs	T_{rr}	--	25	--	ns
Reverse Recovery Charge		Q_{rr}	--	12	--	nC

Note:
1. Pulse width≤100μs, duty cycle≤2%
2. Essentially independent of operating temperature typical characteristics
3. Guaranteed by design,not test in mass production
4. $R_{\theta JA}$ and $R_{\theta Jc}$ are the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 $inch^2$ with 2oz.square pad of copper.
5. The test condition is L=0.1mH, I_{AS}=5.6A, V_{DD}=30V, V_{GS}=10V, Starting T_J=25°C.

Switching Time Waveform

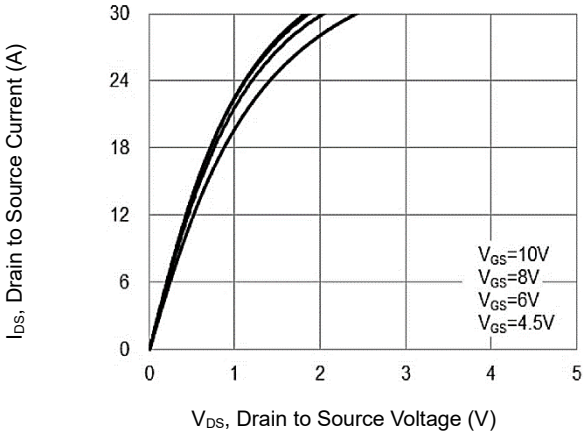


Switching Test Circuit

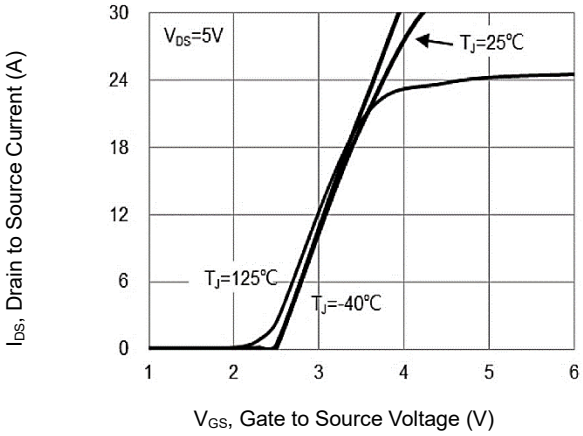


CHARACTERISTIC CURVES

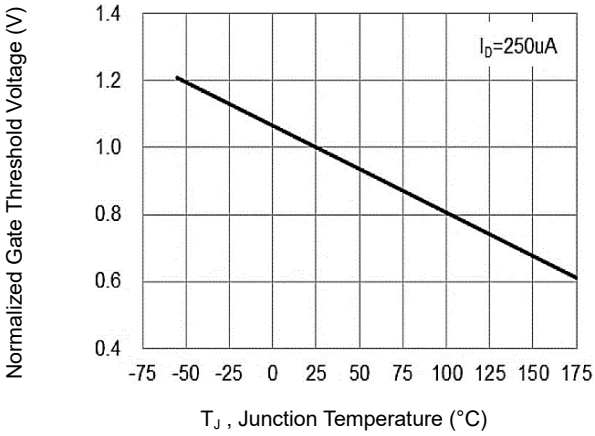
On-Region Characteristics



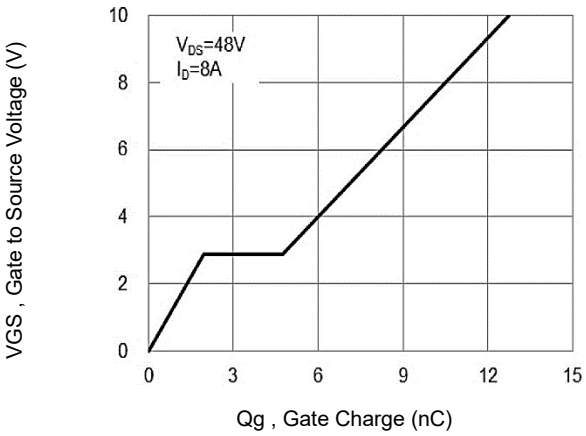
Transfer Characteristics



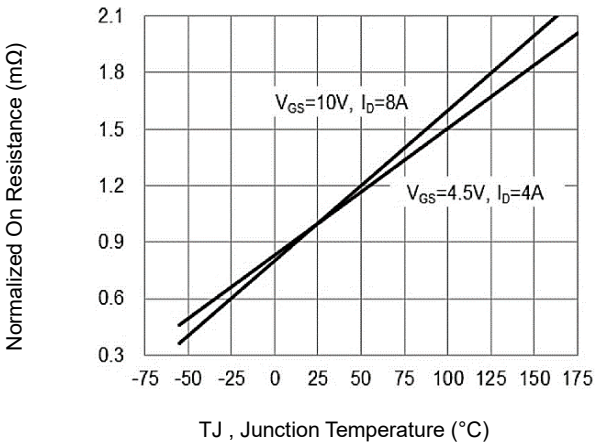
Normalized V_{th} vs. T_J



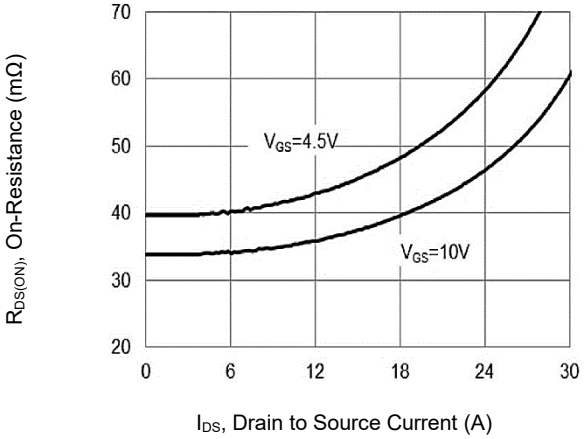
Gate Charge Waveform



Normalized $R_{DS(ON)}$ vs. T_J

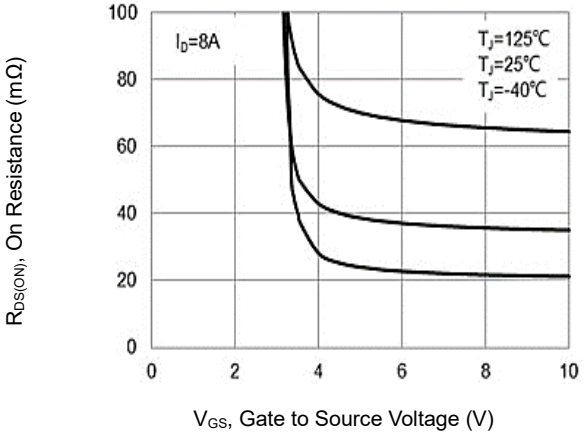


On-Resistance vs. Drain Current

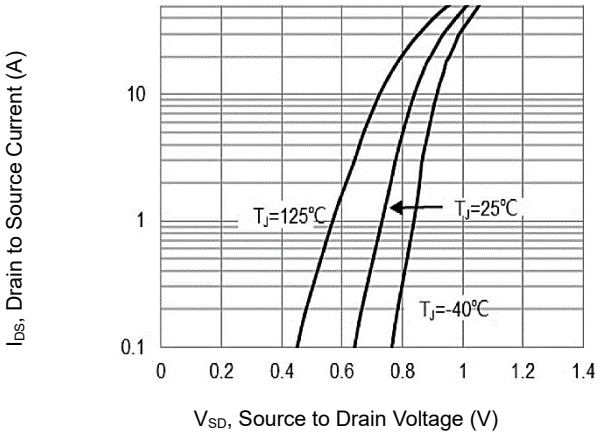


CHARACTERISTIC CURVES

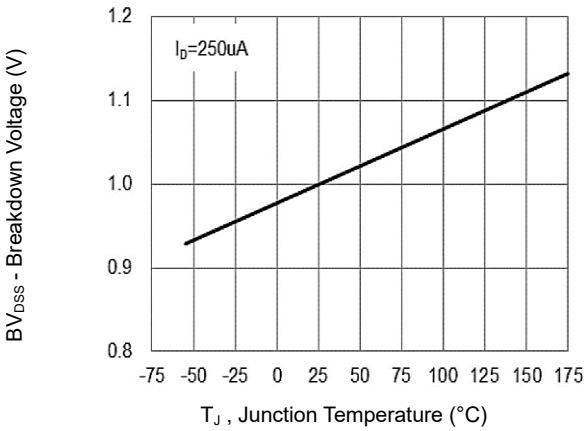
On-Resistance Variation with V_{GS}



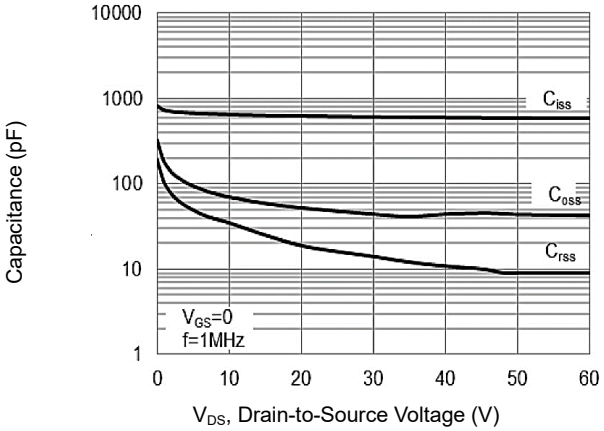
Body Diode



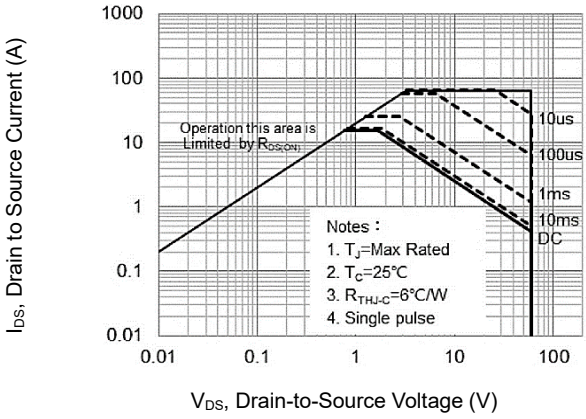
Breakdown Voltage vs Junction Temperature



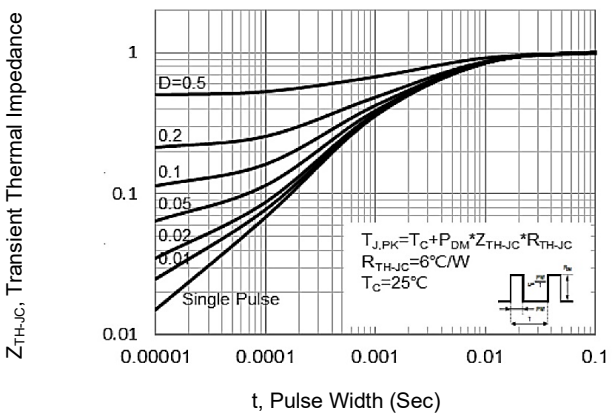
Capacitance vs. Drain-Source Voltage



Maximum Safe Operating Area



Normalized Transient Thermal Impedance



DIMENSIONS

DFN5×6-8L	Min (mm)	Max (mm)
A	0.90	1.10
b	0.33	0.51
C	0.20	0.30
D	4.80	5.00
D2	3.61	3.96
E	5.90	6.10
E1	5.70	5.80
E2	3.38	3.78
e	1.27	
L	0.51	0.71
L1	0.06	0.20
H	0.41	0.61
P	1.56	1.73