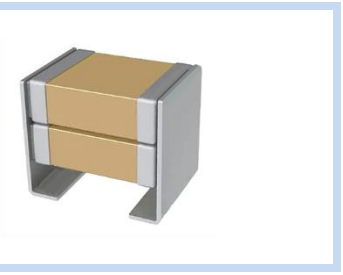
Multilayer Ceramic Chip Capacitors
Stack type AEC-Q200

HA Series

MERITEK

FEATURE

- **A Wide Selection Of Sizes are Available (1210 to 2225)**
- **High Reliability and Stability**
- **Higher Mechanical Endurance**
- **Improved Vibration Performance**
- **Application: DC to DC converter, Power supplies, High Voltage coupling/DC blocking, Back-lighting Inverters, Surge Protection, Snubbers in High Frequency Power Converters, Filtering, Smoothing and Decoupling Application**



PART NUMBERING SYSTEM

HA	2H	X	225	M	451	LL	G
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)

RoHS

No	Item	Code	Description	
(1)	**Meritek Series**	HA	Multilayer Ceramic Chip Capacitor, Stack type, AEC-Q200	
(2)	**Size Code**	2H	2H: 2 chips, size 2220	See dimension table below
(3)	**Dielectric**	X	X: X7R	N: C0G(NP0)
(4)	**Capacitance**	225	225: 22x10^{5}pF = 2.2μF	First two digits: significant, Third: multiplier
(5)	**Tolerance**	M	M: ±20%	See capacitor tolerance table below
(6)	**Rated Voltage**	451	451: 450VDC	First two digits: significant; Third: multiplier
(7)	**Package, Lead**	LL	L: TR , L: L type Lead	See Packaging and Lead type Table below
(8)	**Thickness**	G	G: 6.60±0.35 mm	See thickness table below

ELECTRICAL CHARACTERISTICS

Properties	Characteristics	
Dielectric	C0G(NP0)	X7R
Chip Size	1210, 1812, 1825, 2220, 2225	1210, 1812, 1825, 2220, 2225
Rated Voltage	50V, 100V, 200V, 250V, 500V, 630V	50V, 100V, 200V, 250V, 500V, 630V
Capacitance Range	220nF Max.	47μF Max.
Capacitance Tolerance	See Capacitance Tolerance Reference Table Below	
Dissipation Factor (Tan δ)	**Cap. Range** / **Q Spec**: Cap<30pF: Q≥400+20C; Cap≥30pF: Q≥1000	**Cap. Range** / **DF Spec**: 1210≥3.3μF: D.F.≤5.0%; 1812~2225≥10μF: D.F.≤5.0%; Other: D.F.≤2.5%
Test Condition for Dissipation Factor and Capacitance	**Cap. Range** / **Test Condition**: Cap<1000pF: 1.0±0.2Vrms, 1.0MHz±10%; Cap≥1000pF: 1.0±0.2Vrms, 1.0KHz±10%. For 25°C at ambient temperature	**Cap. Range** / **Test Condition**: Cap≤10uF: 1.0±0.2Vrms,; Cap>10uF: 0.5±0.2Vrms, 120Hz±20%. Preconditioning for Class II MLCC: Perform a heat treatment at 150±10°C for 1 hour, then leave in ambient condition for 24±2 hours before measurement
Insulation Resistance	≥10GΩ or R•C≥500Ω-F Whichever is smaller	≥10GΩ or R•C≥100Ω-F Whichever is smaller
Operation Temperature	-55 ~ +125°C	-55 ~ +125°C
Temperature Coefficient	±30ppm/^{0}C	±15%
Termination	L/J/ Straight type lead	L/J/ Straight type lead

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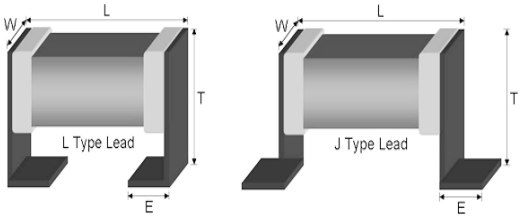
CAPACITANCE RANGE - (1210~ 2225)

Chip Size	Size Code	C0G (NP0) Dielectric						X7R Dielectric					
		50V	100V	200V	250V	500V	630V	50V	100V	200V	250V	500V	630V
1210	1A	393	223	103	103	103	103	475	335	684	684	104	104
1812	1C	104	473	273	273	223	223	106	475	105	105	474	224
	2C	224(M)	104	563	563	473(M)	473(M)	226(M)	106	225(M)	225(M)	105	474(M)
1825	1G	104	104	683	683	473	223	106	106	105	105	564	564
	2G	224(M)	224(M)	134	134	104	473(M)	226(M)	226(M)	225(M)	225(M)	125(M)	125(M)
2220	1H	104	104	683	683	473	223	226	106	225	225	474	474
	2H	224(M)	224(M)	134	134	104	473(M)	476(M)	226(M)	475(M)	475(M)	105	105
2225	1I	104	104	104	104	823	683	106	106	275	275	564	564
	2I	224(M)	224(M)	224(M)	224(M)	184(M)	134	226(M)	226(M)	565	565	125(M)	125(M)

Note: Contact Meritek for other options

EXTERNAL DIMENSIONS

Chip Size	Code	L (mm)	W (mm)	T (mm)	E (mm)
1210	A	3.50±0.40	2.50±0.40	See Thickness Specification Reference Table below	1.70±0.15
1812	C	4.80±0.40	3.20±0.40		1.70±0.15
1825	G	4.80±0.40	6.30±0.50		1.70±0.15
2220	H	6.00±0.50	5.00±0.50		1.70±0.15
2225	I	6.00±0.50	6.30±0.50		1.70±0.15



CAPACITANCE TOLERANCE REFERENCE

Code	Description	Code	Description	Code	Description	Code	Description
A	±0.05 pF	G	±2 %	L	0%~10%	Z	-20%~80%
B	±0.10 pF	H	±3 %	M	±20 %	X	+10% ~ +20%
C	±0.25 pF	I	-10%~0%	N	-5%~10%	--	--
D	±0.50 pF	J	±5 %	P	±0.02 pF	--	--
F	±1 %	K	±10 %	Q	±0.03 pF	--	--

THICKNESS SPECIFICATION REFERENCE

Code	T (mm)	Code	T (mm)	Code	T (mm)	Code	T (mm)
A	3.00 ± 0.35	G	6.60 ± 0.35	M	9.60 ± 0.35	S	12.60 ± 0.35
B	3.60 ± 0.35	H	7.20 ± 0.35	N	10.20 ± 0.35	T	13.20 ± 0.35
C	4.20 ± 0.35	I	--	O	--	U	1.70 ± 0.25
D	4.80 ± 0.35	J	7.80 ± 0.35	P	10.80 ± 0.35	V	2.10± 0.25
E	5.40 ± 0.35	K	8.40 ± 0.35	Q	11.40 ± 0.35	W	2.50± 0.25
F	6.00 ± 0.35	L	9.00 ± 0.35	R	12.00 ± 0.35	X	--

PACKAGE AND LEAD TYPE

Code	Package Type
L	T/R: 13” Reel, Embossed Tape
T	Tray Package
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Code	Lead Type	Code	Lead Type
L	L lead	K	K lead
J	J lead	B	B lead
S	Straight	F	Straight

APPLICATION NOTES

STORAGE

- To prevent the damage of solderability of terminations, the following storage conditions are recommended:
  Indoors under 5ºC~ 40ºC and 20% ~ 70% RH.
  No harmful gases containing sulfuric acid, ammonia, hydrogen sulfide or chlorine.
- Packaging should not be opened until the capacitors are required for use. If opened, the pack should be re-sealed as soon as is practicable. Taped product should be stored out of direct sunlight, which might promote deterioration in tape or adhesion performance. The product is recommended to be used within 6 months and checked the solderability before use.

HANDLING

- Chip capacitors are dense, hard, brittle, and abrasive materials. They are liable to suffer mechanical damage, in the form of cracks or chips. Chip Capacitors should be handled with care to avoid contamination or damage. To use vacuum or plastic tweezers to pick up or plastic tweezers is recommended for manual placement. Tape and reeled packages are suitable for automatic pick and placement machine.

PREHEAT

- In order to minimize the risk of thermal shock during soldering, a carefully controlled preheat is required. The rate of preheat should not exceed 3℃ per second. c.

SOLDERING

- Use middy activated rosin RA and RMA fluxes do not use activated flux. The amount of solder in each solder joint should be controlled to prevent the damage of chip capacitors caused by the stress between solder, chips, and substrate.

- Hand soldering with temperature-controlled iron not exceeding 30 watts and diameter of tip less than 1.2 mm is recommended, tip of iron should not contact the ceramic body directly, and the temperature of iron should be set to not more than 260℃.

- For bigger chips such as 1210, 1808, 1812, 2211, 2220 and 2225, etc. wave soldering and hand soldering are no recommended.

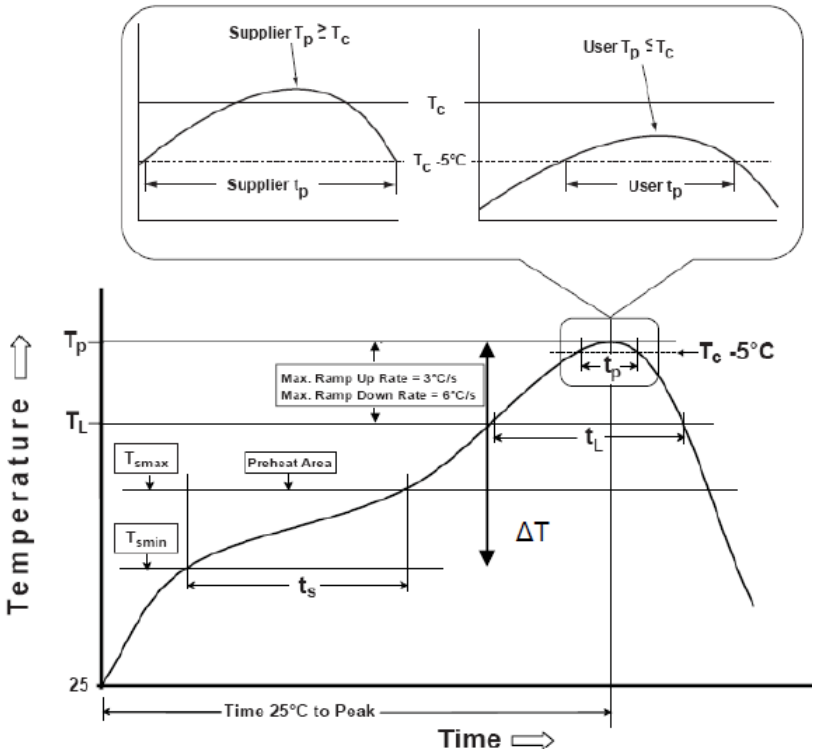
- Refer IPC/JEDEC J-STD-020D Method recommended soldering profiles:
  Reflow not sooner than 15 minutes and not longer than 4 hrs after removal from the temperature/humidity chamber, subject the sample to 3 cycle of the appropriate reflow conditions as the table description below.

Profile Feature		Pb-Free Assembly
Preheat/Soak	Temperature MIN (T_{smin}) Temperature MAX. (T_{SMAX}) Time(t_s) from (T_{smin} to T_{smax})	150ºC 200ºC 60~120 seconds
Ramp-up rate (T_L to T_P)		3^0C/second max.
Liquidous Temperature (T_L) Time(T_L) maintained above T_L		217^0C 60~150 seconds
Peek package body temperature(T_P)		For user T_p must not exceed the classification temp 260^0C For supplier T_p must equal or exceed the classification temp 260^0C
Time(T_P)* within 5^0C of the specified classification temperature(T_C)		30 seconds
Ramp-down rate (T_P to T_L)		6ºC/second MAX.
Time 25^0C to peak temperature 260^0C		8 minutes MAX.

- **Lead-free: Soldering temperature = 235 to 260℃, depending on product.**
- **Maximum temperature = Minimum temperature (235℃) + ΔT+ Tolerance for oven process and measurement (5 ~ 7℃)**
- **Time at peak temperature = 10sec, Dwell above 217℃ = 90sec, Ramping rate = 3℃/sec (heating) and 6℃/sec (heating).**

APPLICATION NOTES (CONTINUED)

CLASSIFICATION REFLOW PROFILES



Chip Size	ΔT
0805, 1206	100°C
1210,1808, 1812, 1825, 2211, 2220, 2225	50°C

Soldering	Solder Temp. (T_C)	Soldering Time (t_p)
Reflow	235~260°C	< 15sec.

Note:
For example: Tc is 260℃ and time t_p is 15sec.
For user: The peak temperature must not exceed 260℃. The time above 255℃ must not exceed 15 seconds.

COOLING

- After soldering, cool the chips and the substrate gradually to room temperature. Natural cooling in air is recommended to minimize stress in the solder joint.

CLEANING

- All flux residues must be removed by using suitable electronic-grade vapor-cleaning solvents to eliminate contamination that could cause electrolytic surface corrosion. Good results can be obtained by using ultrasonic cleaning of the solvent. The choice of the proper system is depends upon many factors such as component mix, flux, and solder paste and assembly method. The ability of the cleaning system to remove flux residues and contamination from under the chips is very important.