

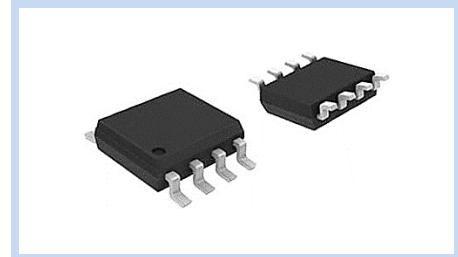
Dual N-Channel MOSFET 60V 4.1A 2W SOP-8

MFT62N4A1S8

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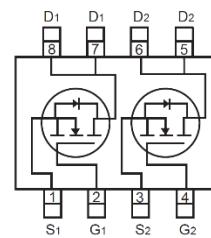
FEATURE

- $R_{DS(ON)} < 68m\Omega$, V_{GS} at 10V
- $R_{DS(ON)} < 86m\Omega$, V_{GS} at 4.5V
- Super High Dense Cell Design for Extremely Low $R_{DS(ON)}$
- High Power and Current Handling Capability



MECHANICAL DATA

- Case: SOP-8 Package
- Terminals: Solderable per MIL-STD-750, Method 2026

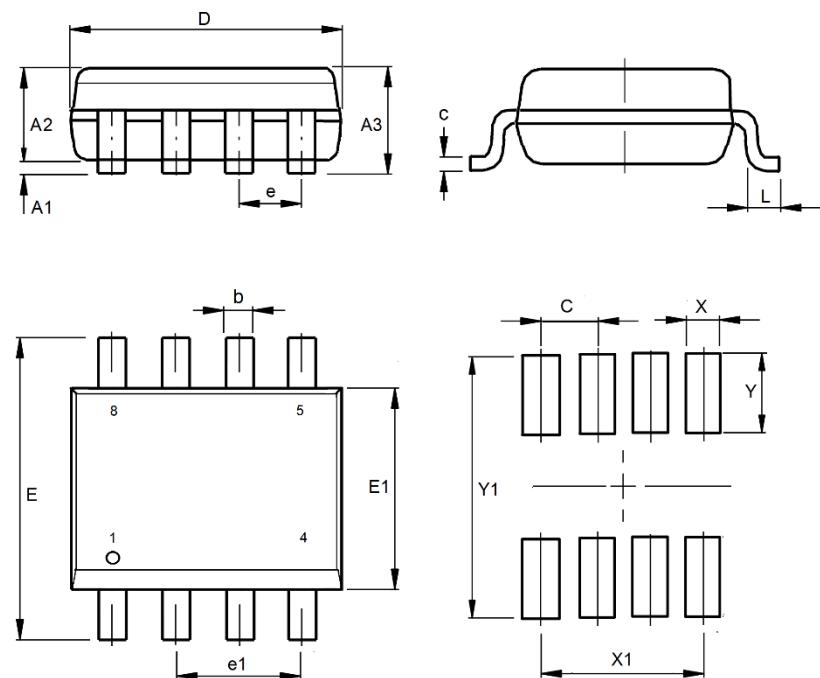


MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current – Continuous	I_D	4.1	A
Drain Current – Pulsed	I_{DM}	16.4	A
Maximum Power Dissipation	P_D	2	W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

DIMENSIONS AND PIN LAYOUT

SOP-8	Min. (mm)	Max. (mm)
A	1.35	1.75
A1	0.10	0.25
A2	1.25	1.50
A3	1.35	1.75
b	0.31	0.51
c	0.17	0.25
D	4.69	5.00
E	5.80	6.20
E1	3.70	4.06
e	1.27 BSC	
h	0.25	0.50
L	0.40	0.95
X	0.5	
X1	3.81	
Y	1.0	
Y1	6.75	
C	1.27	



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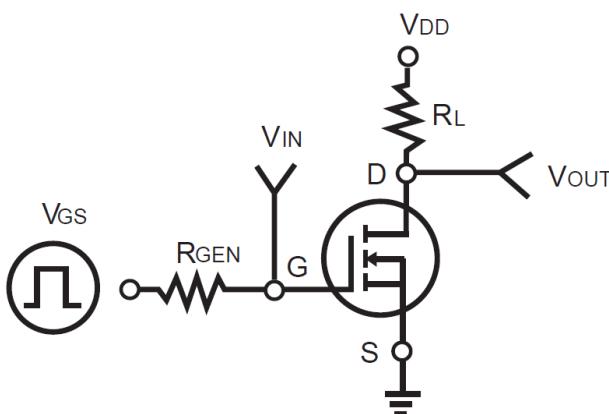
ELECTRICAL CHARACTERISTICS

Static Characteristics	Conditions	Symbol	Min	Typ.	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D= 250\mu A$	$V_{(BR)DSS}$	60	--	--	V
Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	$V_{GS(th)}$	1	--	3	
Gate Leakage Current, Forward	$V_{DS}=0V, V_{GS}= 20V$	I_{GSSF}	--	--	100	nA
Gate Leakage Current, Reverse	$V_{DS}=0V, V_{GS}= -20V$	I_{GSSR}	--	--	-100	nA
Zero Gate Voltage Drain Current	$V_{DS}= 60V, V_{GS}=0V$	I_{DSS}	--	--	1	μA
Drain-Source On-Resistance	$V_{GS}=10V, I_D= 4.1A$	$R_{DS(ON)}$	--	57	68	$m\Omega$
	$V_{GS}=4.5V, I_D= 3.5A$		--	67	86	
Diode Forward Voltage	$I_S=1.5A, V_{GS}=0V$	V_{SD}	--	--	1.2	V
Diode Forward Current	--	I_S	--	--	1.5	A
Dynamic Characteristics	Conditions	Symbol	Min	Typ.	Max	Unit
Total Gate Charge	$V_{DS}= 30V, V_{GS}= 10V, I_D= 4.1A$	Q_g	--	13.2	17.6	nC
Gate-Source Charge		Q_{gs}	--	1.2	--	
Gate-Drain Charge		Q_{gd}	--	4.1	--	
Input Capacitance	$V_{DS}= 25V, V_{GS}= 0V, f=1.0MHz$	C_{iss}	--	530	--	pF
Output Capacitance		C_{oss}	--	70	--	
Reverse Transfer Capacitance		C_{rss}	--	50	--	
Turn-On Delay Time	$V_{DD}=30V, I_D \geq 1A, V_{GS}=10V, R_{GEN}=6\Omega$	$t_{d(on)}$	--	9	18	nS
Turn-On Rise Time		t_r	--	4	8	
Turn-Off Delay Time		$t_{d(off)}$	--	28	56	
Turn-Off Rise Time		t_f	--	3	6	

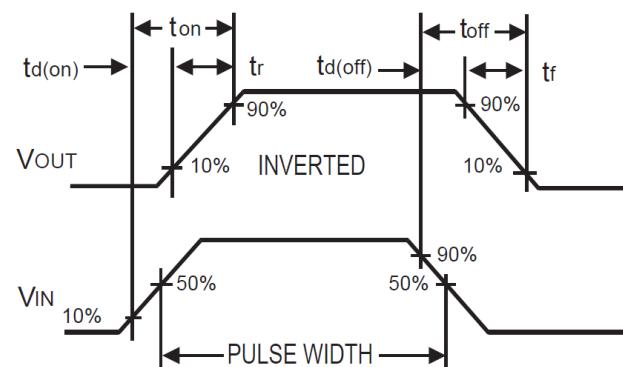
Notes:

1. Pulse Test, Pulse Width<300 μS , Duty Cycle<2%
2. Surface Mounted on FR4 Board, t<10Sec
3. Repetitive Rating : Pulse width limited by maximum junction temperature
4. $T_A=25^\circ C$ unless otherwise specified
5. Guaranteed by design, not subject to production testing.

Switching Test Circuit



Switching Waveforms



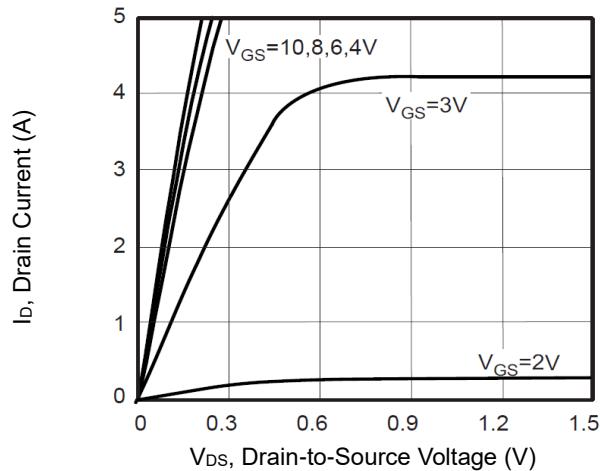
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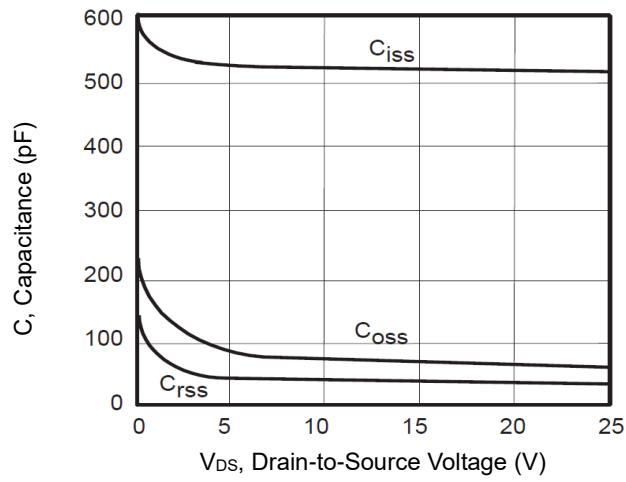
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CHARACTERISTIC CURVES

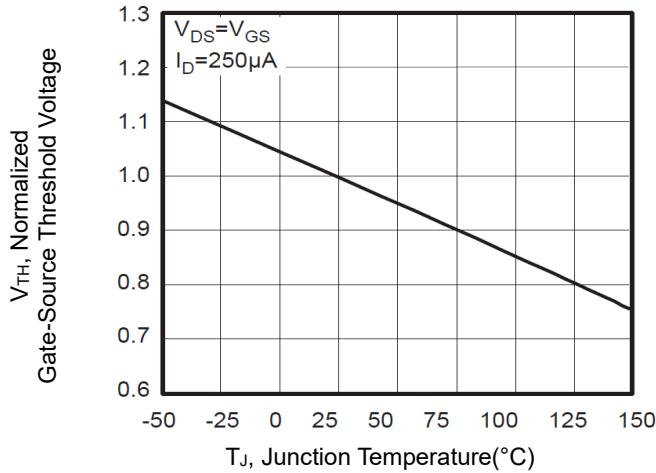
Output Characteristics



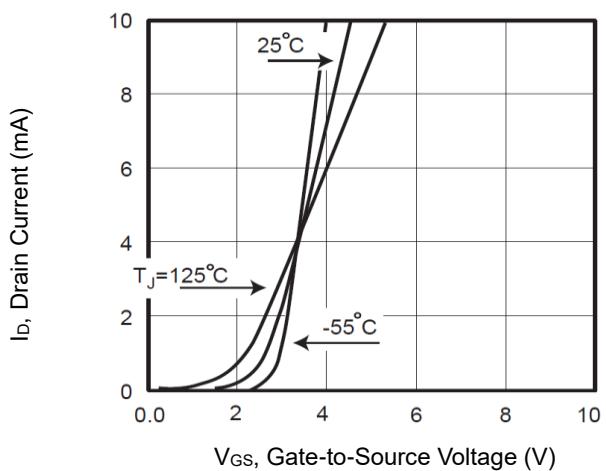
Capacitance



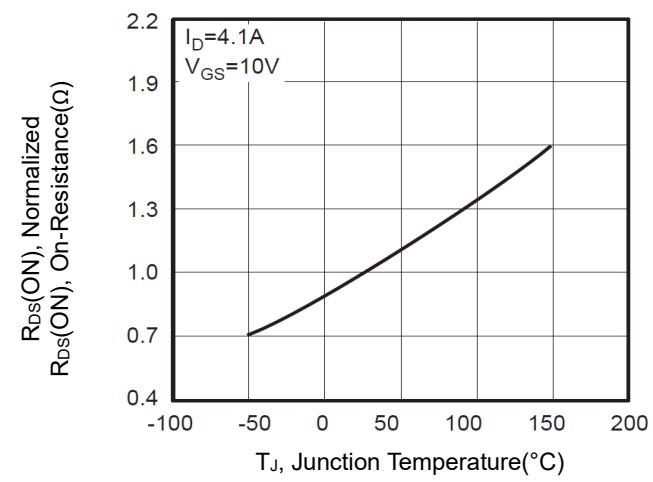
Gate Threshold Variation
with Temperature



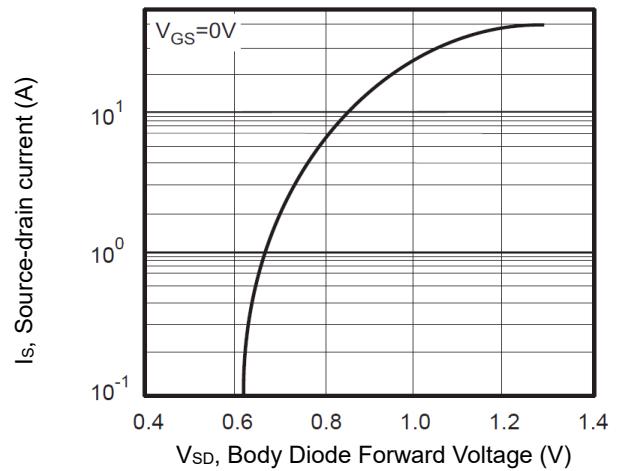
Transfer Characteristics



On-Resistance Variation with Temperature



Body Diode Forward Voltage
Variation with Source Current



Dual N-Channel MOSFET

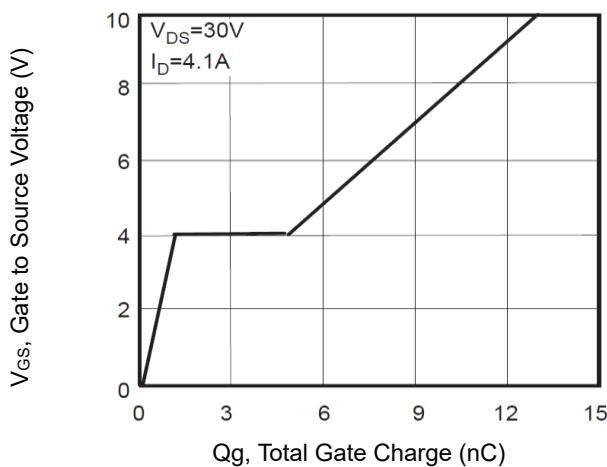
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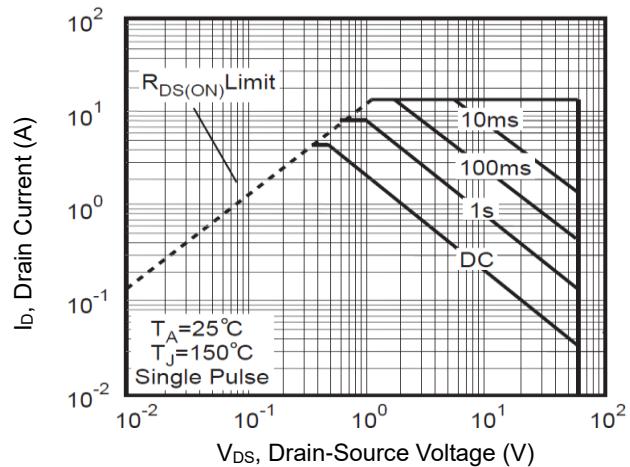
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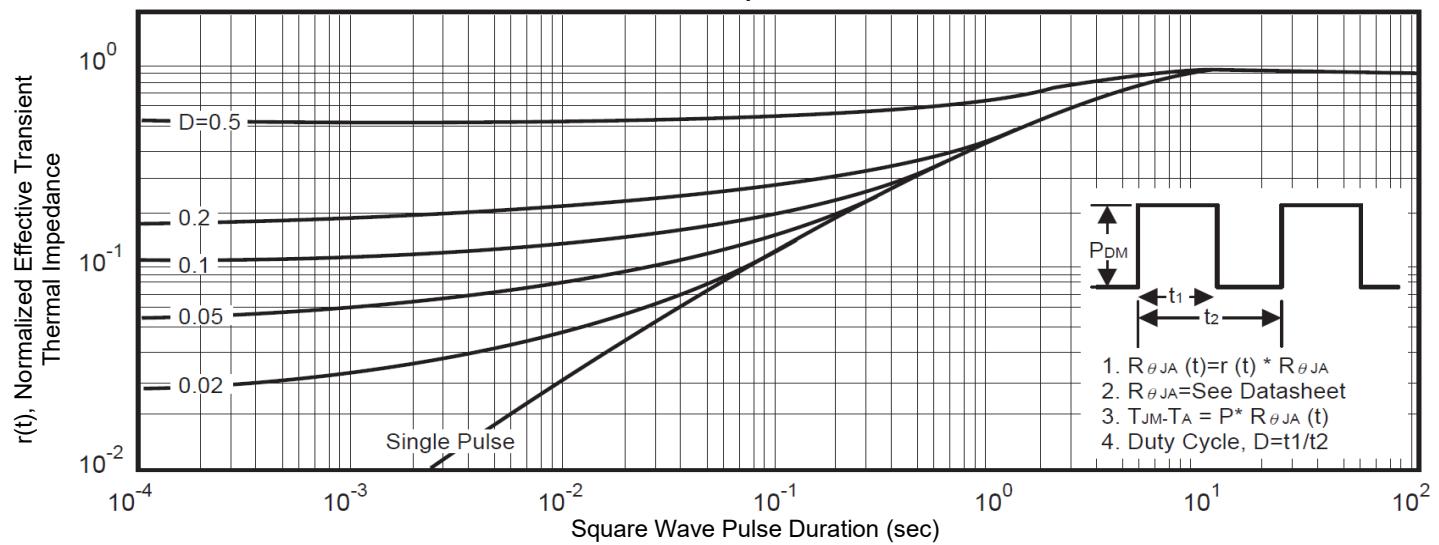
Gate Charge



Maximum Safe Operating Area



Normalized Thermal Transient Impedance Curve, Junction-to-Ambient



*Specifications subject to change without notice.