

N-Channel MOSFET

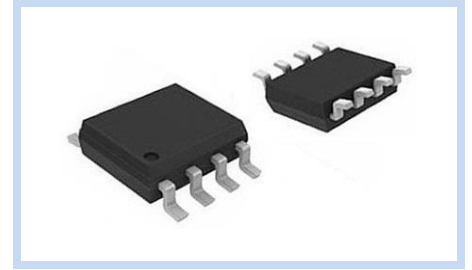
100V 7.0A SOP-8

MFT10N7A0S8S

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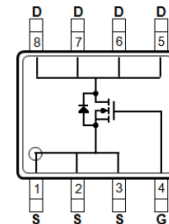
FEATURE

- $R_{DS(ON)} < 25m\Omega$, $V_{GS}=10V$, $I_D=7.0A$
- $R_{DS(ON)} < 28.5m\Omega$, $V_{GS}=4.5V$, $I_D=5.0A$
- High density cell design for ultra low on-resistance
- Advanced Trench Process Technology
- Lead free in compliance with EU RoHS



MECHANICAL DATA

- Case: SOP-8 package
- Terminal: Solderable per MIL-STD-750, Method 2026

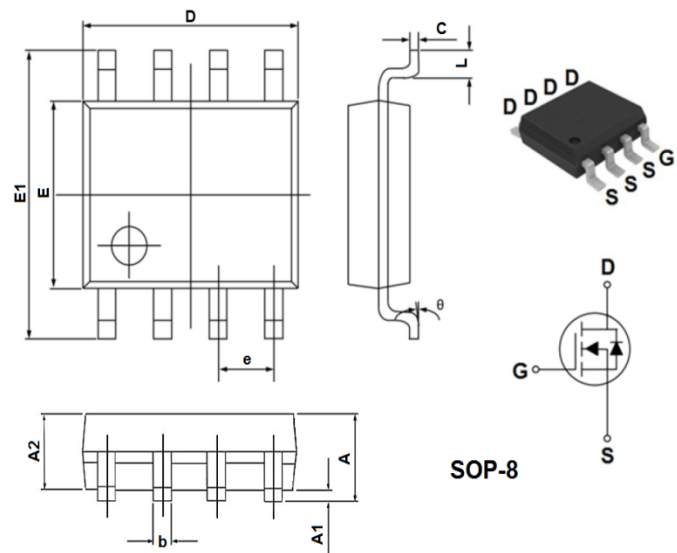


MAXIMUM RATINGS (TA=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current – Continuous	I_D	$T_C=25^\circ C$	7.0
		$T_C=70^\circ C$	5.6
Drain Current – Pulsed	I_{DM}	28	A
Power Dissipation	P_D	$T_C=25^\circ C$	2.5
		$T_C=70^\circ C$	1.6
Single Pulse Avalanche Energy	E_{AS}	8.5	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$
Thermal Resistance Junction to Ambient, $t \leq 10s$	$R_{\theta JA}$	50	$^\circ C/W$

DIMENSIONS AND PIN LAYOUT

Item	Min. (mm)	Max. (mm)
A	1.35	1.75
A1	0.10	0.25
A2	1.30	1.50
b	0.31	0.51
c	0.17	0.25
D	4.80	5.00
E	3.80	4.00
E1	5.80	6.20
e	1.27 BSC	
L	0.40	1.27
θ	0°	8°



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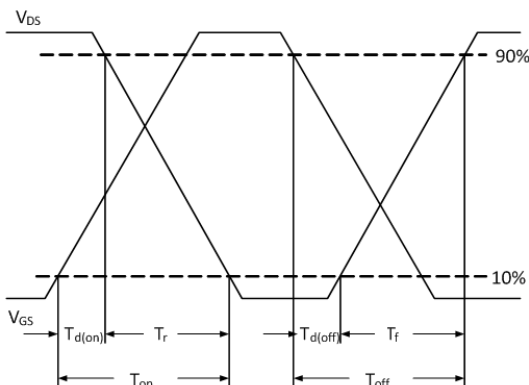
ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

Static Characteristics	Conditions	Symbol	Min	Typ.	Max	Unit
Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	BV _{DSS}	100	--	--	V
Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250μA	V _{GS(th)}	1.0	1.8	2.5	V
Drain-Source On-Resistance	V _{GS} =10V, I _D =7.0A	R _{DS(ON)}	--	20	25	mΩ
Drain-Source On-Resistance	V _{GS} =4.5V, I _D =5.0A	R _{DS(ON)}	--	22	28.5	mΩ
Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V	I _{DSS}	--	--	1.0	μA
Gate-Source Leakage Current	V _{DS} =0V, V _{GS} =±8V	I _{GSS}	--	--	±100	μA
Dynamic Characteristics	Conditions	Symbol	Min	Typ.	Max	Unit
Input Capacitance	V _{DS} =30V, V _{GS} =0V, F=1.0MHz	C _{iss}	--	1519	--	pF
Output Capacitance		C _{oss}	--	132	--	pF
Reverse Transfer Capacitance		C _{rss}	--	66	--	pF
Switching Characteristics	Conditions	Symbol	Min	Typ.	Max	Unit
Total Gate Charge	V _{DS} =50V, V _{GS} =10V, I _D =7.0A	Q _g	--	31	--	nC
Gate-Source Charge		Q _{gs}	--	5.1	--	
Gate-Drain Charge		Q _{gd}	--	7.3	--	
Turn-On Delay Time	V _{DD} =50V, V _{GS} =10V, R _G =3Ω I _D =7.0A	T _{d(on)}	--	11	--	ns
Turn-On Rise Time		T _r	--	42	--	
Turn-Off Delay Time		T _{d(off)}	--	40	--	
Turn-Off Fall Time		T _f	--	19	--	
Drain-Source Body Diode	Conditions	Symbol	Min	Typ.	Max	Unit
Drain-Source Diode Forward Current	--	I _S	--	--	7.0	A
Drain-Source Diode Forward Voltage	V _{GS} =0V, I _S =1.0A	V _{SD}	--	0.7	1.2	V

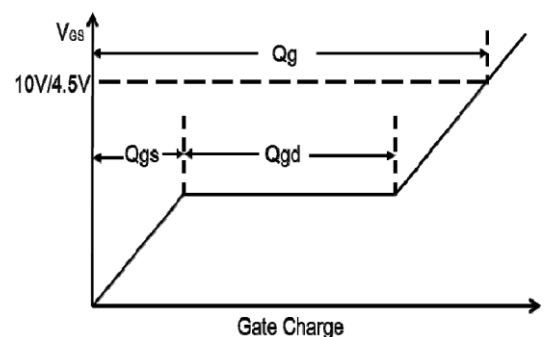
Note:

1. Pulse width ≤ 300μs, duty cycle ≤ 2%
2. Essentially independent of operating temperature typical characteristics
3. The maximum current rating is package limited.
4. Repetitive rating, pulse width limited by junction temperature T_J(MAX)=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J = 25°C.
5. The test condition is L=0.1mH, I_{AS}=13A, V_{DD}=50V, V_{GS}=10V
6. R_{θJA} is the sum of the junction to case to ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins mounted on a 1inch FR-4 with 2oz. square pad of copper.
7. Guaranteed by design, not subject to production testing.

Switching Time Waveform



Gate Charge Waveform



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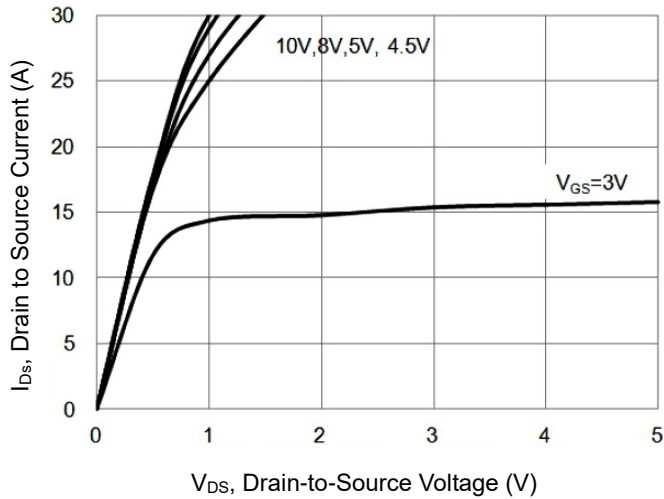
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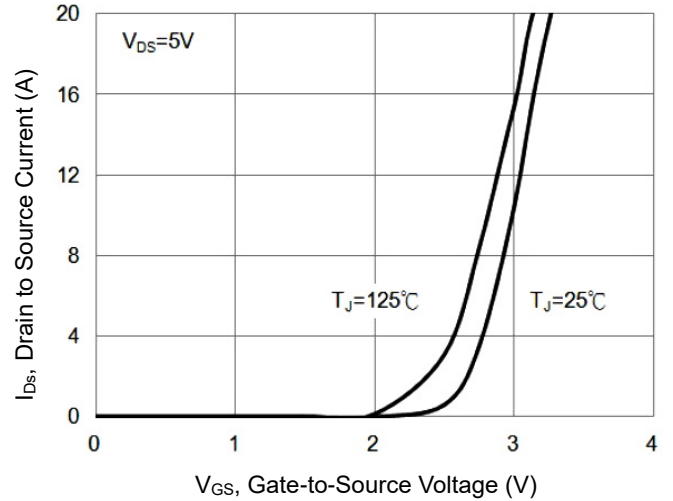
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CHARACTERISTIC CURVES

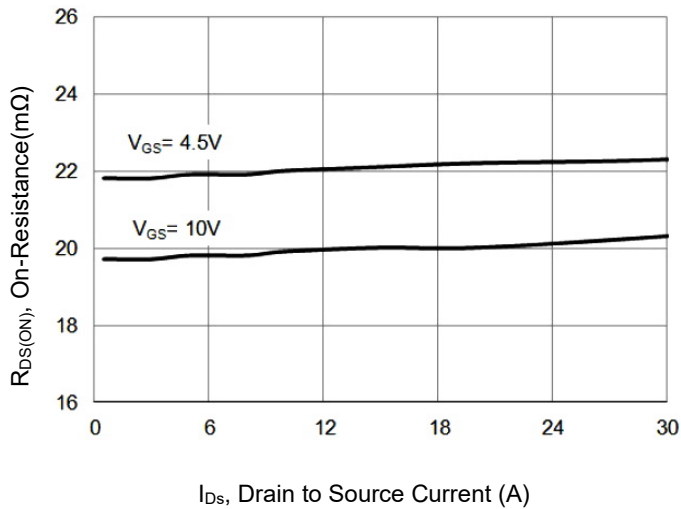
On-Region Characteristics



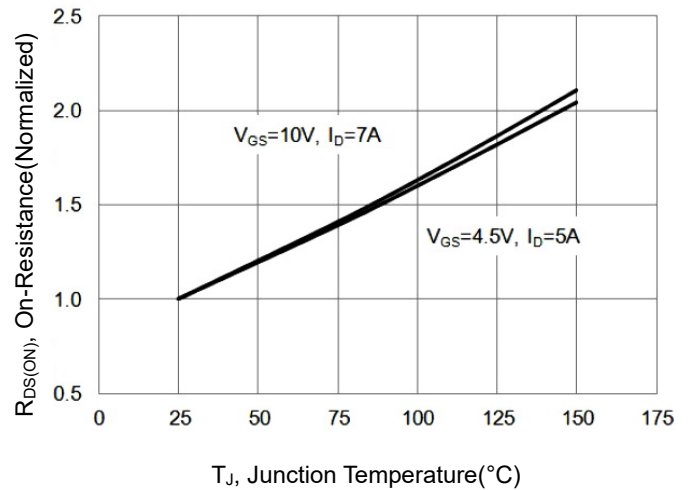
Transfer Characteristics



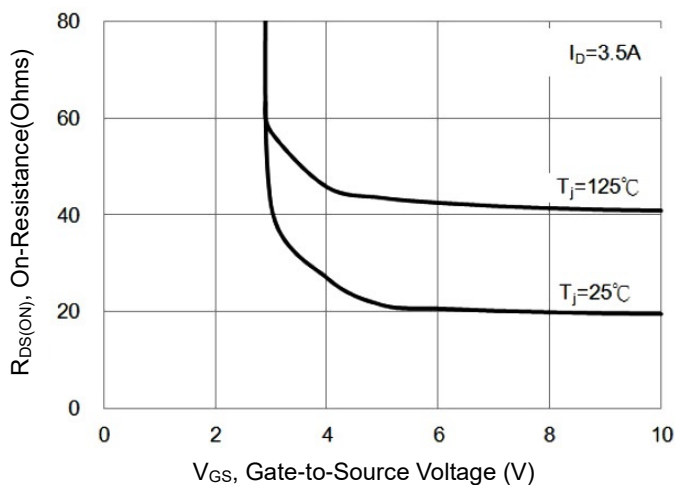
On-Resistance Variation vs. Drain Current



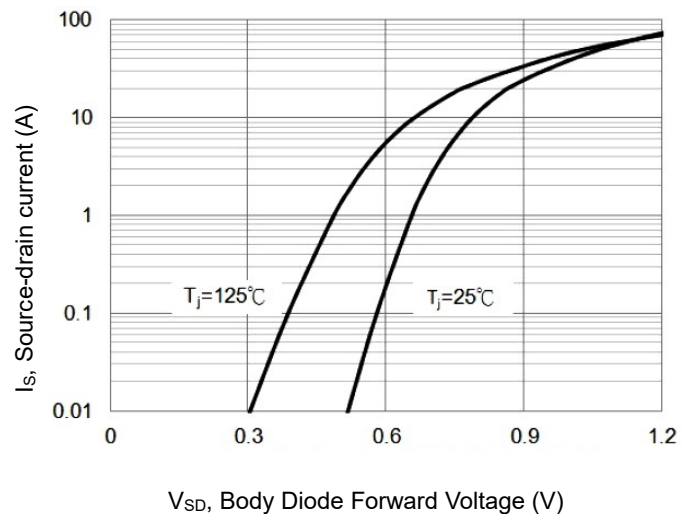
On-Resistance Variation vs. Temperature



On-Resistance Variation vs. Vgs



Body Diode Characteristics



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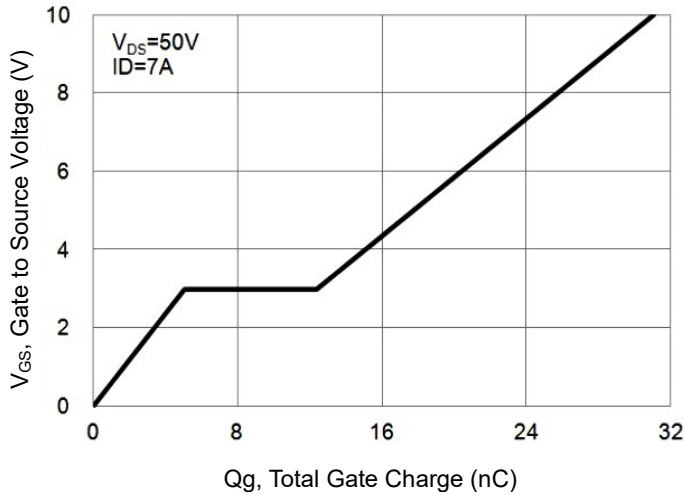
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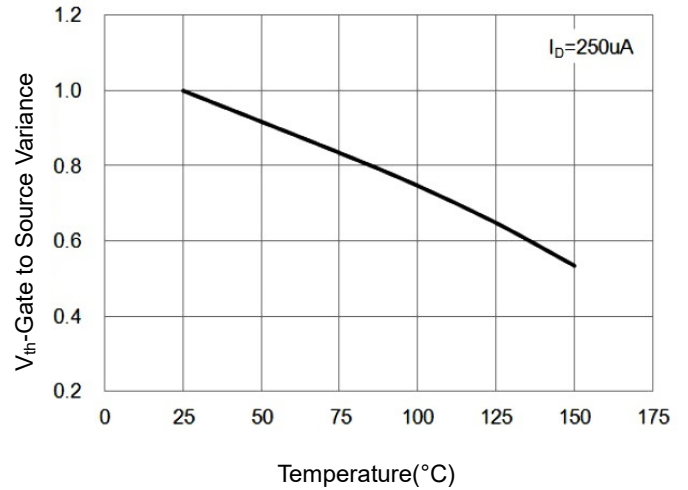
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CHARACTERISTICS CURVES (CONTINUED)

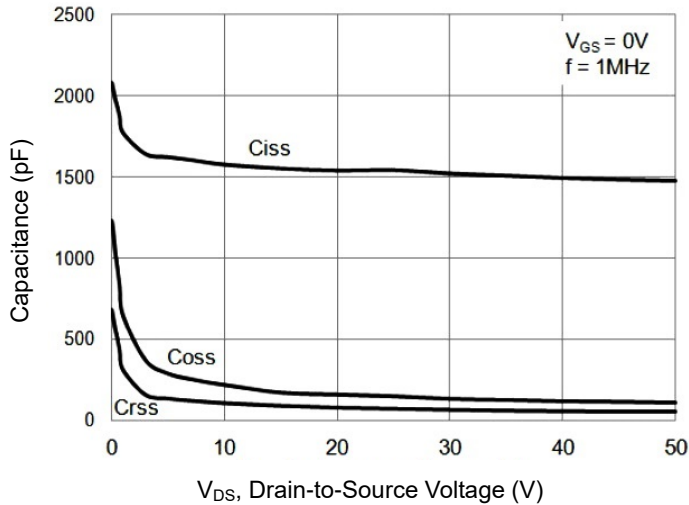
Gate Charge Characteristics



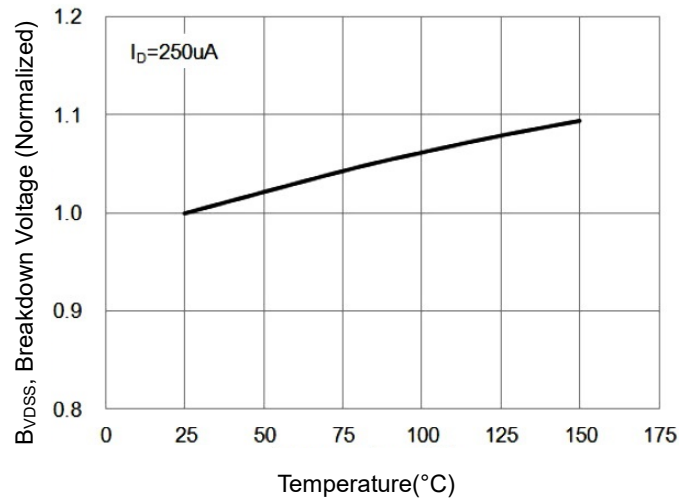
Threshold Voltage Variation with Temperature



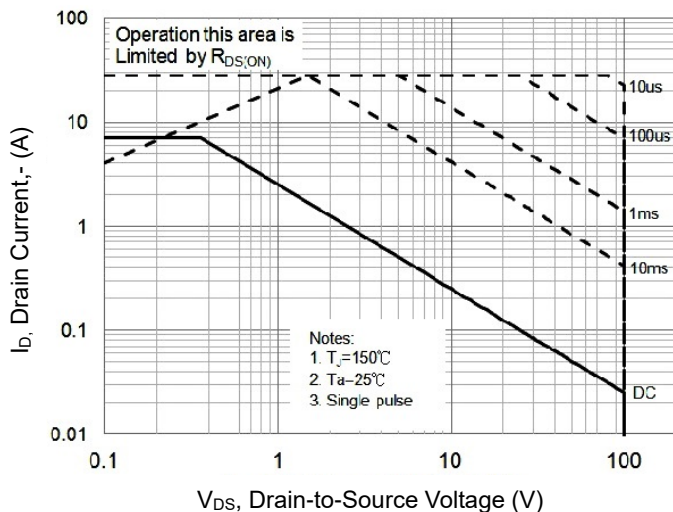
Capacitance vs. Drain Source Voltage



Breakdown Voltage Variation vs. Temperature



Maximum Safe Operating Area



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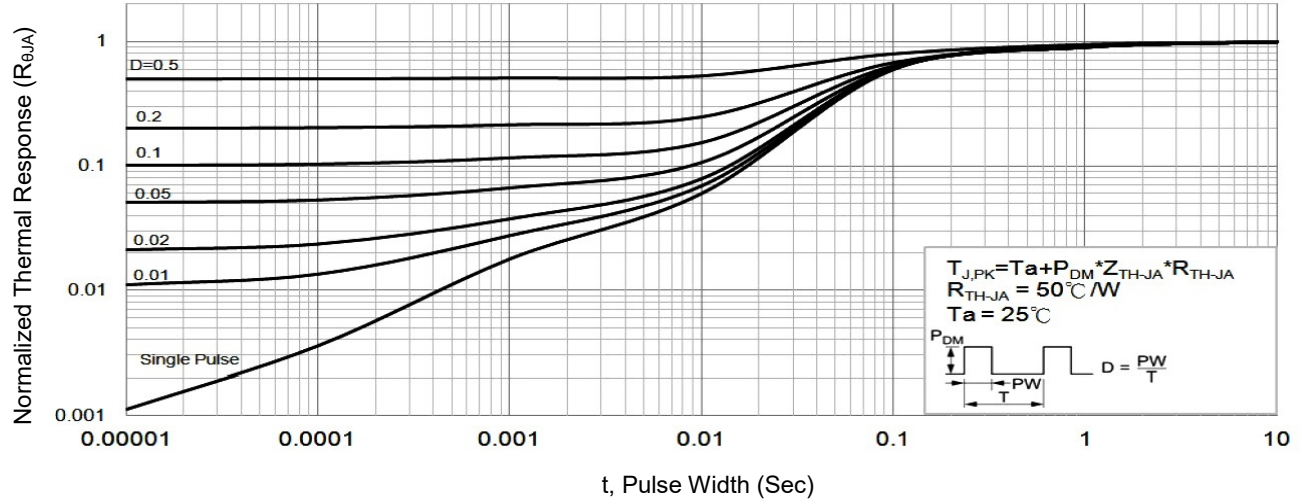
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CHARACTERISTICS CURVES (CONTINUED)

Normalized Transient Thermal Impedance vs. Pluse Width



*Specifications subject to change without notice.