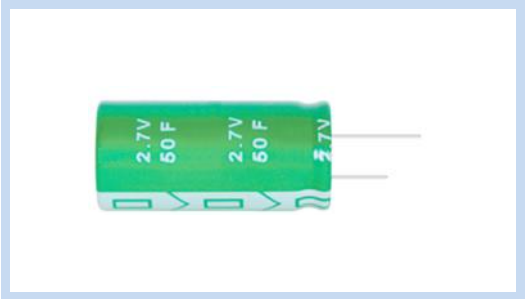
Super Capacitors – EDLC
Low ESR Type

SCE-R series

MERITEK

FEATURES

- **Operating Temperature Range: -40°C ~ +60°C**
- **Load life of 1000 hours at 60°C**
- **High capacitance and high temperature**
- **Applications: Consumer electronics, Industrial and automation, portable power tools, renewable energy storage systems, and short term UPS (uninterruptible power supply)**



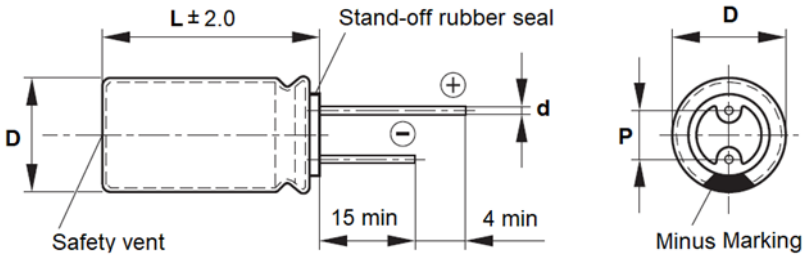
PART NUMBERING SYSTEM

RoHS

SC	E	304	M	27	D11	R
(1)	(2)	(3)	(4)	(5)	(6)	(7)

No	Item	Digit	Description	Series Reference
(1)	**Meritek Series**	SC	Super Capacitors series	Radial Leaded Type
(2)	**Product Type**	E	E: Low ESR Type	1000 Hours 60°C
(3)	**Capacitance**	304	304: 0.3F, 300,000	335: 3.3F, 506: 50F, 107:100F
(4)	**Tolerance**	M	M: ±20%	-20%~+20%
(5)	**Rated Voltage**	27	27: 2.7 VDC	Rated Voltage
(6)	**Case Size**	D11	D11: 4x 11mm	Diameter X Length mm
(7)	**Internal Code**	R	R: Radial type	Lead type or project reference

DIMENSIONS – Radial type



Radial type	4	8 (L<20)	8(L>20)	10	12.5	16	18
Code	**D**	**H**	**H**	**J**	**K**	**L**	**M**
D±0.5	**4**	**8**	**8**	**10**	**12.5**	**16**	**18**
P	2.5	3.5	3.5	5	5	7.5	7.5
ϕ d±0.05	0.5	0.5	0.6	0.6	0.6	0.8	0.8

ELECTRICAL SPECIFICATIONS

SCE-R Series	Rated Capacitance	Tolerance	Rated Voltage	Surge Voltage	ESR DC max	ESR AC max 1KHz/20°C	Leakage Current
	(F)	(%)	(VDC)	(VDC)	(mΩ)	(mΩ)	(mA/72hrs)
SCE304M27D11R	0.3	±20%	2.7	2.8	1500	1000	0.006
SCE105M27H12R	1.0	±20%	2.7	2.8	850	400	0.008
SCE205M27H16R	2.0	±20%	2.7	2.8	470	280	0.01
SCE305M27H20R	3.0	±20%	2.7	2.8	250	160	0.012

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	(F)	(%)	(VDC)	(VDC)	(mΩ)	(mΩ)	(mA/72hrs)
SCE335M27J20R	3.3	±20%	2.7	2.8	270	160	0.014
SCE475M27J20R	4.7	±20%	2.7	2.8	250	140	0.016
SCE705M27J25R	7.0	±20%	2.7	2.8	200	100	0.02
SCE106M27J30R	10	±20%	2.7	2.8	130	80	0.03
SCE106M27K25R	10	±20%	2.7	2.8	140	80	0.03
SCE226M27L25R	22	±20%	2.7	2.8	85	40	0.06
SCE306M27L30R	30	±20%	2.7	2.8	60	30	0.07
SCE506M27M40R	50	±20%	2.7	2.8	40	25	0.16
SCE107M27M60R	100	±20%	2.7	2.8	28	20	0.3

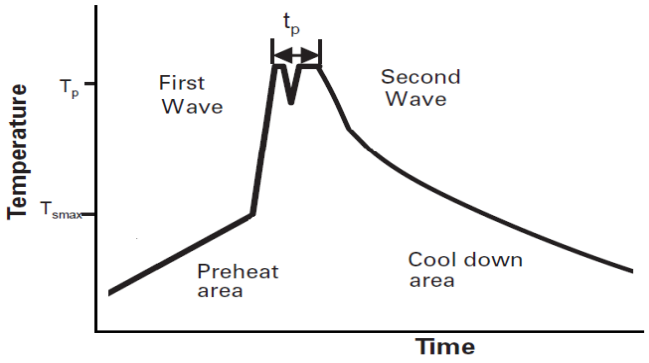
SCE-R Series	Short Circuit Current	Max. Continuous Current	Max. Peak Current	Power Density	Energy Density	Maximum Energy	Size DxL
	(A)	(A) T= 15˚C	(A) (Isc)	(W/Kg)	(Wh/Kg)	(mAh)	(mm)
SCE304M27D11R	18	0.2	0.5	2333	1.2	0.31	4 x 11
SCE105M27H12R	3.17	0.4	0.73	1338	1.3	1.01	8 x 12
SCE205M27H16R	5.74	0.5	1.39	1756	1.9	2.03	8 x 16
SCE305M27H20R	10.8	0.8	2.31	2647	2.3	3.04	8 x 20
SCE335M27J20R	10	08	2.36	1580	1.6	3.34	10 x 20
SCE475M27J20R	10.8	0.9	2.92	1645	2.2	4.76	10 x 20
SCE705M27J25R	13.5	1	3.94	1934	3.1	7.09	10 x 25
SCE106M27J30R	20.7	1.4	5.87	2057	3.1	10.1	10 x 30
SCE106M27K25R	19.3	1.4	5.63	1755	2.8	10.1	12.5 x 25
SCE226M27L25R	31.7	2.1	10.3	1650	3.6	22.3	16 x 25
SCE306M27L30R	45	2.7	14.5	1768	3.7	30.4	16 x 30
SCE506M27M40R	67.5	4	225	1770	4.1	50.6	18 x 40
SCE107M27M60R	96.4	5.8	35.5	1625	5.3	101	18 x 60

RELIABILITY TEST CONDITON AND REQUIREMENT

Item	Characteristic	
Endurance	After 1,000 hours application of rated voltage at +60°C, the capacitor shall meet the following limits.	
	Capacitance Change	≤ ±30% of initial value
	Internal Resistance	≤ 2 times of initial specified value
Cycles	Capacitor cycles between specified voltage and half rated voltage under constant current at +25°C (25000 cycles)	
	Capacitance Change	≤ ±30% of initial value
	Internal Resistance	≤ 2 times of initial specified value

RECOMMENDED SOLDERING PROFILES

Wave Soldering		
Pre Heat and Soak	Temperature Max $T_{s(max)}$	100°C
	Time (min. to max.) (t_s)	60sec max
Preheat to Max Temperature		160°C max
Peak Temperature (T_P)		220~260°C
Time to Peak Temperature T_P (t_p)		10s Max, 5s Each wave
Ramp-down Rate		~5 K/s max
Time 25°C to 25°C		4 min



Solder Exposure Time

Solder Bath	Recommended	Maximum
220°C	7sec	9sec
240°C	7sec	9sec
250°C	5sec	7sec
260°C	3sec	5sec

Note:
Use a maximum preheating time of 60 seconds
for PC boards 0.8mm or thicker.
Preheating temperature should be limited to less than 100˚C.

APPLICATION NOTE

1. **Life Time**
   EDLC has a longer life time than secondary batteries, but their life time is not infinite. The basic end-of- life failure mode for an EDLC is an increase in equivalent series resistance (ESR) and/or a decrease in capacitance. The actual end-of-life criteria are dependent on the application requirements. Prolonged exposure to elevated temperatures, high applied voltage and excessive current will lead to increased ESR and decreased capacitance. Reducing these parameters will lengthen the life time of a supercapacitor. In general, cylindrical EDLC have a similar construction to electrolytic capacitors, they have a liquid electrolyte inside an aluminum can sealed with a rubber bung. Over many years, the EDLC will dry out, similar to an electrolytic capacitor, causing an increase in ESR and eventually end-of-life

2. **Voltage**
   EDLC are rated with a nominal recommended working or applied voltage. The values provided are set for long life at their maximum rated temperature. If the applied voltage exceeds the recommended voltage, the life time will be reduced. If the applied voltage is excessive for a prolonged time period, gas generation will occur inside the EDLC and may result in leakage or rupture of the safety vent. However, short-term over voltage can usually be tolerated by the EDLC.

3. **Polarity**
   EDLC are designed with symmetrical electrodes, meaning they are similar in composition. When an EDLC is first assembled, either electrode can be designated positive or negative. Once the EDLC is charged for the first time during the 100% QA testing operation, the electrodes become polarized. Every EDLC has a negative stripe or sign denoting polarity. Although they can be shorted to zero volts, the electrodes maintain a very small amount of charge. Reversing polarity is not recommended, however previously charged EDLC have been discharged to –2.5V with no measurable difference in capacitance or ESR.

4. **Ripple Current**
   EDLC have a very low resistance compared to other supercapacitors but have a higher resistance than aluminum electrolytic capacitors. EDLC are more suDRptible to internal heat generation when exposed to ripple current. In order to ensure long life time, the maximum ripple current recommended should not increase the surface temperature of the EDLC by more than 3˚C, as heat generation leads to electrolyte decomposition, gas generation, increased ESR and reduced life time.

5. **Ambient Temperature**

The standard temperature range is –25˚C to +70˚C for SCT series or –40˚C to +60˚C for SCE series. Temperature in combination with voltage can affect the life time of an EDLC. In general, raising the ambient temperature by 10˚C will decrease the life time of an EDLC by a factor of two. As a result, it is recommended to use the EDLC at the lowest temperature possible to decrease internal degradation and ESR increase. At temperature lower than normal room temperature, it is possible to apply voltages slightly higher than the recommended working voltage without significant increase in degradation and reduction in life time. Raising the applied voltage at low temperatures can be useful to offset the increased ESR. Increased ESR at higher temperatures will result in permanent degradation/electrolyte decomposition inside the EDLC. At low temperatures, however, increased ESR is only a temporary phenomenon due to the increased viscosity of the electrolyte and slower movement of the ions.

6. **Discharge Characteristics**

EDLC discharges with a sloping voltage curve. When determining the capacitance and ESR requirements for an application, it is important to consider both the resistive and capacitive discharge components. In high current pulse applications, the resistive component is the most critical. In low current and long duration applications, the capacitive discharge component is the most critical.

The formula for the voltage drop, Vdrop, during a discharge at I current for t seconds is:

Vdrop = I (R+t/C)

To minimize voltage drop in a pulse application, use an EDLC with low ESR (R value).
To minimize voltage drop in a low current application, use an EDLC with large capacitance (C value).

7. **Charge Methods**

EDLC can be charged using various methods including constant current, constant power, constant voltage or by paralleling to an energy source, i.e. battery, fuel cell, DC converter, etc. If an EDLC is configured in parallel with a battery, adding a low value resistor in series will increase the life of the battery. If a series resistor is used, ensure that the voltage outputs of the EDLC are connected directly to the application and not through the resistor; otherwise the low ESR of the EDLC will be nullified. Many battery systems exhibit decreased life time when exposed to high current discharge pulses.

The maximum recommended charge current I, for an EDLC where Vw is the charge voltage and R is the EDLC ESR is calculated as below: **I = Vw/5R**
Overheating of the EDLC can occur from continuous overcurrent or overvoltage charging. Overheating can lead to increased ESR, gas generation, decreased life time, leakage, venting or rupture. Contact the factory if you plan to use a charge current or voltage higher than specified.

8. **Self-Discharge and Leakage Current**

Self-discharge and leakage current is essentially the same thing measured in different ways. Due to the EDLC construction, there is a high-resistance internal current path from the anode to the cathode. This means that in order to maintain the charge on the capacitor a small amount of additional current is required. During charging this is referred to as leakage current. When the charging voltage is removed, and the capacitor is not loaded, this additional current will urge the EDLC to discharge and is referred to as the self-discharge current.

In order to get a realistic measurement of leakage or self-discharge current the EDLC must be charged for an excess of 100 hours. This is also due to the capacitor construction. The EDLC can be modeled as several capacitors connected in parallel, each with an increasing value of series resistance. The capacitors with low values of series resistance are charged quickly thus increasing the terminal voltage to the same level as the charge voltage. However, if the charge voltage is removed these capacitors will discharge into the parallel capacitors with higher series resistance if they are not fully charged. The result of this is that the terminal voltage will fall, giving the impression of high self-discharge current. It should be noted that the higher the capacitance value is, the longer it will take for the device to be fully charged.

9. **Series Configurations of EDLC**

Individual EDLC are limited to 2.5V for SCT series or 2.7V for SCE series. As many applications require higher voltages, EDLC can be configured in series to increase the working voltage. It is important to ensure that the individual voltage of any single EDLC does not exceed its maximum recommended working voltage as this will result in electrolyte decomposition, gas generation, increased ESR and reduced life time.

Capacitor voltage imbalance is caused, during charge and discharge, by differences in capacitance value and, in steady state, by differences in capacitor leakage current. During charging, series connected capacitors will act as a voltage divider so higher capacitance devices will receive greater voltage stress. For example, if two 1F capacitors are connected in series, one at +20% of nominal capacitance, the other at –20%, the worst-case voltage across the capacitors is given by:

Vcap2 = Vsupply x (Ccap1/(Ccap1+Ccap2)) where Ccap1 has the +20% capacitance.
So for a Vsupply = 5V, **Vcap2 = 5V x (1.2/(1.2+0.8)) = 3V**

From above, it can be seen that in order to avoid exceeding the EDLC surge voltage rating of 3V , the capacitance values of series connected parts must fall in a ±20% tolerance range. Alternatively a suitable active voltage balancing circuit can be employed to reduce voltage imbalance due to capacitance mismatch. It should be noted that the most appropriate method of voltage balancing depends on the specific application.

10. Passive Voltage Balancing

Passive voltage balancing uses voltage-dividing resistors in parallel with each EDLC. This allows current to flow from the EDLC at a higher voltage level into the EDLC at a lower voltage level, thus balancing the voltage. It is important to choose balancing resistors values that provide for higher current flow than the anticipated leakage current of the EDLC, bearing in mind that the leakage current will increase at higher temperatures.

Passive voltage balancing is only recommended for applications that don't regularly charge and discharge the EDLC and that can tolerate the additional load current of the balancing resistors. It is suggested that the balancing resistors be selected to give additional current flow of at least 50 times the worst-case EDLC leakage current (3.3kΩ to 22kΩ depending on maximum operating temperature). Although higher values of balancing resistors will work in most cases they are unlikely to provide adequate protection when significantly mismatched parts are connected in series.

11. Active Voltage Balancing

Active voltage balancing circuits force the voltage at the nodes of series connected EDLC to be the same as a fixed reference voltage, regardless of how many voltage imbalances occur. To ensure accurate voltage balancing, active circuits typically draw much lower levels of current in steady state and only require larger currents when the capacitor voltage goes out of balance. These characteristics make active voltage balancing circuits ideal for applications that charge and discharge the EDLC frequently as well as those with a finite energy source such as a battery.

12. Reverse Voltage Protection

When series connected EDLC are rapidly discharged, the voltage on low capacitance value parts can potentially become negative. As explained previously, this is not desirable and can reduce the operating life of the EDLC. One simple way of protecting reverse voltage is to add a diode across the capacitor, configured so that it is normally reverse bias. By using a suitably rated zener diode in place of a standard diode the EDLC can also be protected against overvoltage events. Care must be taken to ensure that the diode can withstand the available peak current from the power source.

13. Soldering Information

Excessive heat may cause deterioration of the electrical characteristics of the EDLC, electrolyte leakage or an increase in internal pressure. Follow the specific instructions listed as below:

- Do not dip EDLC body into melted solder.
- Only flux the leads of the EDLC.
- Ensure that there is no direct contact between the sleeve of the EDLC and the PC board or any other component. Excessive solder temperature may cause sleeve to shrink or crack.
- Avoid exposed circuit board runs under the EDLC to prevent electrical shorts.

14. Circuit Board Design

Cleaning of the circuit board should be avoided. If the circuit board must be cleaned use static or ultrasonic immersion in a standard circuit board cleaning fluid for no more than 5 minutes and a maximum temperature of +60˚C. Afterwards thoroughly rinse and dry the circuit boards. In general, treat EDLC in the same manner you would an aluminum electrolytic capacitor.

15. Long Term Storage

Do not store EDLC in any of the following environments:

- High temperature and/or high humidity
- Direct contact with water, salt water, oil or other chemicals
- Direct contact with corrosive materials, acids, alkalis or toxic gases
- Direct exposure to sunlight
- Dusty environment
- Environment subject to excessive shock and/or vibration

*Specifications subject to change without notice.