

Multilayer Ceramic Chip Capacitor Array

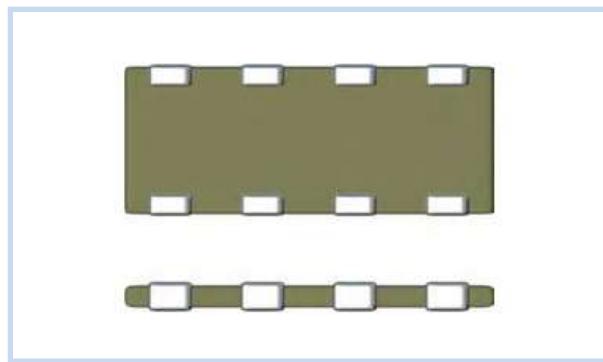


CI Series

MERITEK

FEATURES

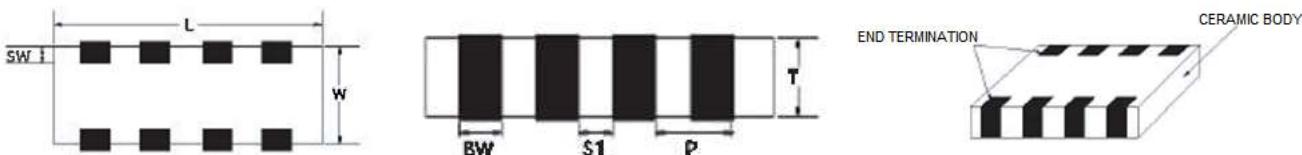
- Reduction in required real estate (more than 50%)
- Reduced cost, space and time for placement on PCB
- Reduction in number of solder joints
- Easier PCB design
- Reduced waste from tape and reel packaging process
- Protect EMI bypassing digital signal line noise



APPLICATION

- For use as bypass for digital and analog signal line noise
- Computer motherboards and peripherals
- The other common electronic circuits

STRUCTURE AND DIMENSION



Type	Element	L (mm)	W (mm)	T (mm)		BW(mm)	SW(mm)	S1 (mm)	P (mm)
0805 (2012)	4	2.00±0.15	1.25±0.15	0.85±0.10	T	0.25±0.10	0.20±0.10	0.25±0.10	0.50±0.10
1206 (3216)	4	3.20±0.15	1.60±0.15	0.80±0.10	B	0.40±0.15	0.3±0.20	0.40±0.20	0.80±0.15

PART NUMBERING SYSTEM

Meritek Series, C-array	CI	1206	XR	101	K	500
	Size					
Dielectric						
CODE		CG	XR	YV		
COG (NP0)		X7R		Y5V		
Capacitance						
CODE	8R2	101	104	223		
pF	8.2	100	--	--		
nF	--	--	100	22		
μF	--	--	0.1	0.022		
Tolerance						
CODE	Tolerance	Code	Tolerance	Code	Tolerance	
B	±.10pF	G	±2%	M	±20%	
C	±.25pF	J	±5%	Z	+80/-20%	
D	±.50pF	K	±10%	P	+1000/0%	
For values less than 10 pF use C or D						
Rated Voltage						
2 significant digits + number of zeros						
CODE	100	160	250	500	101	
R.V.	10V	16V	25V	50V	100V	

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ELECTRICAL SPECIFICATIONS

Dielectric	NPO		X7R				Y5V			
Size	0805		1206		0805		1206			
Capacitance*	10pF to 270pF		10pF to 470pF		1000pF to 100nF		180pF to 100nF			
Capacitance tolerance**	J ($\pm 5\%$), K ($\pm 10\%$)				K ($\pm 10\%$), M ($\pm 20\%$)					
Rated voltage (WVDC)	25V, 50V, 100V		10V, 16V, 25V, 50V		16V, 25V, 50V		16V, 50V			
Tan δ^*	Cap<30pF, Q \geq 400+20C Cap \geq 30pF, Q \geq 1000			Ur=50V, $\leq 2.5\%$ Ur = 25V&16V, $\leq 3.5\%$ Ur=10V, $\leq 5.0\%$			Ur=50V, $\leq 5\%$ Ur=16V, $\leq 7\%$			
Insulation resistance at Ur	$\geq 10G\Omega$			$\geq 10G\Omega$ or $RxC \geq 500\Omega \times F$ whichever is less						
Operating temperature	-55 to +125°C							-25 to +85°C		
Capacitance characteristic	$\pm 30ppm$			$\pm 15\%$				+30~-80%		
Termination	Ni/Sn (lead-free termination)									

* Measured at 30~70% related humidity.

NPO: Apply 1.0 ± 0.2 Vrms, $1.0\text{MHz} \pm 10\%$ at the conditions of 25°C ambient temperature.

X7R: Apply 1.0 ± 0.2 Vrms, $1.0\text{kHz} \pm 10\%$ at the conditions of 25°C ambient temperature.

Y5V: Apply 1.0 ± 0.2 Vrms, $1.0\text{kHz} \pm 10\%$ at the conditions of 20°C ambient temperature.

** Preconditioning for Class II MLCC: Perform a heat treatment at $150 \pm 10^\circ\text{C}$ for 1 hour, then leave in ambient condition for 24 ± 2 hours before measurement.

CAPACITANCE RANGE

SIZE		0805 (4 x 0402)							1206 (4 x 0603)							
DIELECTRIC		NPO			X7R				NPO			X7R			Y5V	
RATED VOLTAGE (VDC)		25	50	100	10	16	25	50	25	50	100	16	25	50	16	50
Capacitance	10 pF(100)	T	T	T					B	B	B					
	15 pF (150)	T	T	T					B	B	B					
	22 pF (220)	T	T	T					B	B	B					
	33 pF (330)	T	T	T					B	B	B					
	47 pF (470)	T	T	T					B	B	B					
	68 pF (680)	T	T	T					B	B	B					
	100 pF (101)	T	T	T					B	B	B					
	150 pF (151)	T	T	T					B	B	B					
	180 pF (181)	T	T	T					B	B	B		B	B		
	220 pF (221)	T	T	T					B	B	B		B	B		
	270 pF (271)	T	T	T					B	B	B		B	B		
	330 pF (331)								B	B	B		B	B		
	470 pF (471)								B	B	B		B	B		
	680 pF (681)												B	B		
	1000 pF (102)				T	T	T	T					B	B		
	1500 pF (152)				T	T	T	T					B	B		
	2200 pF (222)				T	T	T	T					B	B		
	3300 pF (332)				T	T	T	T					B	B		
	4700 pF (472)				T	T	T	T					B	B		
	6800 pF (682)				T	T	T	T					B	B		
	0.010 μF (103)				T	T	T						B	B		B
	0.015 μF (153)				T	T	T					B	B	B	B	
	0.022 μF (223)				T	T	T					B	B	B	B	
	0.03 μF (333)				T	T	T					B			B	
	0.047 μF (473)				T	T	T					B			B	
	0.068 μF (683)				T	T	T					B			B	
	0.10 μF (104)				T	T	T					B			B	

Note: The letter in cell is expressed the symbol of product thickness. T is 0.85 ± 0.10 mm, and B is 0.80 ± 0.10 mm.